

+EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.

SERIAL NO.

TI-14124D.4

div. of 10/649,274

LIST OF DOCUMENTS CITED BY APPLICANT

(Use several sheets if necessary)

APPLICANT

Lee D. Whetsel

FILING DATE

October 20, 2003

GROUP

~~TDD~~ 2133

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

CB	Avra, LaNae, "A VHSIC ETM-BUS Compatible Test and Maintenance Interface", 1987 International Test Conference, Sept. 1-3, 1987, Paper 41.2, pp. 964-971	
	Bhavsar, et al., "Self-Testing by Polynomial Division", Digest of Papers, International Test Conference, 1981, pp.208-216	
	Breuer, Melvin A.; Lien, Jung-Cheun, "A Test and Maintenance Controller for a Module Containing Testable Chips", 1988 International Test Conference, Sept. 12-14, 1988, Paper 27.1, pp. 502-513	
	Dervisoglu, Bulent I., "Using Scan Technology for Debug and Diagnostics in a Workstation Environment", 1988 International Test Conference, Sept. 12-14, 1988, Paper 45.2, pp.976-986	
	El-ziq, et al., "A Mixed-Mode Built-In Self-Test Technique Using Scan Path and Signature Analysis", International Test Conference, Oct. 18-20, 1983, pp. 269-274	
	ETM-Bus Specification, VHSIC Phase 2 Interoperability Standards, December 31, 1985, Version 1.0	
	Haedtke, et al., "Multilevel Self-test for the Factory and Field", Proceedings, Annual Reliability and Maintainability Symposium, 1987	
	Hahn, et al., "VLSI Testing By On-Chip Error Detection", IBM Technical Disclosure Bulletin, Vol. 25, No. 2, July 1982	
	Hudson, et al., "Integrating BIST And Boundary-Scan On A Board", Proceedings of the National Communications Forum, Sept. 30, 1988, pp. 1796-1800	
	Hudson, et al., "Parallel Self-test With Pseudo-Random Test Patterns", International Test Conference, Sept. 1-3, 1987, pp.954-963	
	IBM Technical Disclosure Bulletin, "Bidirectional Double Latch", Vol. 28, No. 1, June, 1985	
	IBM Technical Disclosure Bulletin, "Self-Contained IBM Performance Monitor for a Personal Computer", December, 1988, Vol. 3, No. 7, pp.376-377	
	Intel, "80386 Programmer's Reference Manual 1986", Chapter 12: Debugging, pp. 12-1 - 12-9, 1/18/1988	
	Intel, "Intel386™ DX Microprocessor Data Sheet," Section 2.11: Testability, 1988	
	Intel, "Microprocessor and Peripheral Handbook", 80386 Preliminary, Section 2.11: Testability, 1988	
CB	Joint Test Action Group, Technical Sub-Committee, "A Standard Boundary Scan Architecture", January 1988	

EXAMINER

C. Butt

DATE CONSIDERED

4-15-05

+EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (REV. 7-80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. TI-14124D.4	SERIAL NO. div. of 10/649,274
LIST OF DOCUMENTS CITED BY APPLICANT <i>(Use several sheets if necessary)</i>				APPLICANT Lee D. Whetsel	
				FILING DATE October 20, 2003	GROUP 300 2133
OTHER DOCUMENTS <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>					
CB		Kuban, John R. and Bruce, William C, "Self-Testing the Motorola MC6804P2," IEEE Design & Test, May, 1984, earlier version in International Test Conference Proceedings, October 1983			
		Laurent, "An Example of Test Strategy for Computer Implemented with VLSI Circuits", IEEE International Conference on computer Design: VLSI in Computers, Oct. 7-10, 1985, pp. 679-682			
		Lien, Jung-Cheun; Breuer, Melvin A., "A Universal Test and Maintenance Controller for Modules and Boards", IEEE Transactions on Industrial Electronics, Vol. 36, No. 2, May 1989, pp. 231-240			
		Marlett, et al., "RISP Methodology", Electronic Engineering, February, 1989, pp.45-48			
		Maunder, Colin, and Beenker, Frans, "Boundary-Scan: A Framework for Structured Design-for-Test," paper 30.1, International Test Conference 1987 Proceedings, Sep. 1-3			
		Ohletz, et al., "Overhead in Scan and Self-testing Designs", International Test Conference, 1987, Sep. 1-3, pp. 460-470			
		Ohsawa, et al., "A 60-ns 1-Mbit CMOS DRAM with Built-In self-Test Function", IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 5, October 1987, pp. 663-668			
		Paraskeva, et al., "New Test Structure for VLSI Self-Test: The Structured Test Register", 8030 Electronic Letters, 21 (1985) sept. No. 19, Stenenage, Herts, Great Britain, July 26, 1985			
		Pradhan, M.M., et al., "Circular BIST with Partial Scan," 1988 International Test Conference, Sept. 12-14, 1987, Paper 35.1, pp. 719-727			
		Russell, "The JTAG Proposal and Its Impact On Automatic Test", ATE & Instrumentation Conference, Sept, 1988, pp. 289-297			
		Sabo, et al., "Genesil Silicon Compilation and Design For Testability", IEEE Custom Integrated Circuits Conference, May 12-15, 1986, pp. 416-420			
		Sellers, et al., "Error Detecting Logic for Digital Computers", McGraw-Hill Co., 1968 pp. 207-211			
		van Riessen, R. P., Kerkhoff, H. G., Kloppenburg, A., "Design and Implementation of a Hierarchical Testable Architecture Using the Boundary Scan Standard", Proceedings, 1 st European Test Conference, Paris, France, April 12-14, 1989, pp. 112-118			
		Wagner, "Interconnect Testing With Boundary Scan", International Test Conference Proceedings, 1987, Sep. 1-3, pp. 52-57			
		Wang, et al., "Concurrent Built-In Logic Block Observer (CBILBO)", IEEE International Symposium On Circuits and Systems", May 5-7, 1986, Vol. 3, pp. 1054-1057			
CB		Wang, Laung-Terng; Marhoefer, Michael; McCluskey, Edward, J., "A Self-Test and Self-Diagnosis Architecture for Boards Using Boundary Scan", Proceedings 1 st European Test Conference, Paris, April 12-14, 1989, pp. 119-126			
EXAMINER C. Butt				DATE CONSIDERED 4-15-05	
+EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609: Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.					

+EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.